



## **JITTER PERFORMANCE OF S/PDIF DIGITAL INTERFACE TRANSCEIVERS: IS MEETING STANDARDS ENOUGH?**

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### **INTRODUCTION**

Although the majority of S/PDIF transceivers on the market may meet IEC60958-3 specifications, it has been noted that many such devices are not robust enough to handle system-level issues in end applications.

This is particularly true for timing parameters such as jitter and timing accuracy, typically a more frequent and serious source of system problems than electrical parameters like output voltage level.

As a device interconnection standard, seamless, stable operation with all vendors and applications is vital to the usability of S/PDIF devices.

It is in this regard that the WM8804 and WM8805 from Wolfson Microelectronics excel. These devices offer market-leading jitter performance, allowing error-free operation at the digital audio interface, and providing extremely low jitter clock and data outputs for further processing in the audio system.

The WM8804 and WM8805 are IEC60958-3 compatible digital interface transceivers. The performance of these devices, particularly with regards to jitter tolerance, combined with a low pin count and high level of flexibility, make the WM8804/5 ideal for a wide range of applications in the professional and consumer domains.

## S/PDIF BACKGROUND

The Sony/Philips Digital Interface (S/PDIF) has been in existence in various forms since the late 1980s. The purpose of the interface is to allow the transport of digital audio data between modules such as hi-fi components in a single-channel (optical or electrical), as opposed to PCM's multiple line format (i.e. clock, data, frame). The format has been standardised in the consumer domain in the form of IEC60958-3 (International Electrotechnical Commission, [www.iec.ch](http://www.iec.ch)), and in the professional domain as AES3 and IEC60958-4. While it is not the intention of this paper to discuss the S/PDIF standard in any depth, some detail will be provided on the format of the S/PDIF signal.

## S/PDIF FORMAT

S/PDIF is a serial, bi-phase-mark encoded data stream, where the data is transmitted in frames in order to identify the various components of the bit stream. An S/PDIF frame consists of two sub-frames. Each sub-frame is made up of:

- Preamble – a synchronization pattern used to identify the start of a 192-frame block or sub-frame
- 4-bit Auxiliary Data (AUX)
- 20-bit Audio Data (24-bit when combined with AUX)
- Validity Bit
- User Bit – over 192-frames, this forms a User Data Block
- Channel Bit – over 192-frames, this forms a Channel Status Block
- Parity Bit – used to maintain even parity over the sub-frame (except the preamble)

An S/PDIF Block consists of 192 frames. Channel and User blocks are incorporated within the 192-frame S/PDIF Block. For Consumer mode, only the first 40-frames are used to make up the Channel and User blocks. Figure 1 illustrates the S/PDIF format.

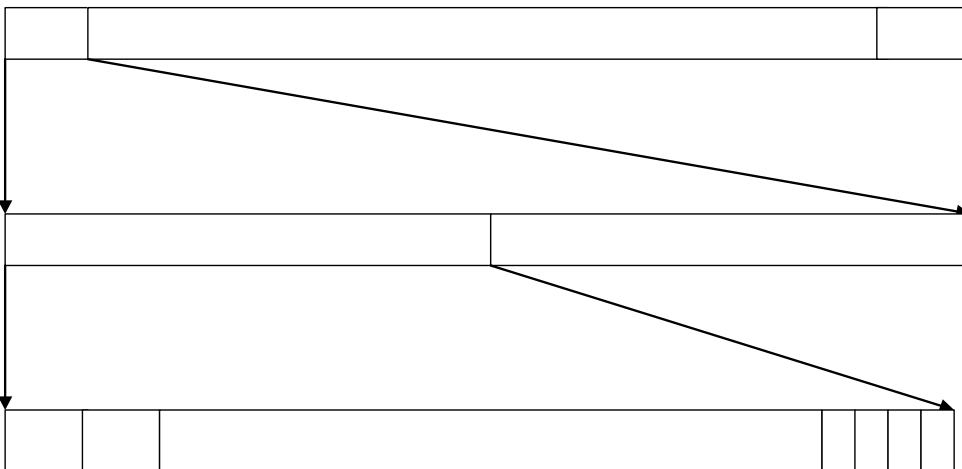


Figure 1 S/PDIF Frame Structure

## **DIGITAL AUDIO SYSTEM RELIABILITY**

Although problems in meeting electrical specifications such as input sensitivity and output level can cause errors in end applications, it has been found that marginal performance in meeting timing parameters is a much more significant contributor to system failure.

IEC-60958-3/4 and AES3 specify a range of timing parameters, including timing accuracy, intrinsic jitter, jitter tolerance, jitter transfer, phase offset and phase tolerance. While it is likely that the majority of commercially available S/PDIF transceivers will meet the necessary standards, it has been found by experimentation that merely meeting standards is not necessarily enough to guarantee overall system performance and stability.

Variations in the stringency of digital audio interface standards mean that meeting one standard does not guarantee seamless interfacing to other standards. This has been especially significant in the professional domain where many products must support multiple digital audio interface types. It will soon become more important in consumer applications where the digital home will support multiple digital sources running simultaneously, with different timing requirements.

Just as important, it has been observed that jitter, in particular, can cause a significant decrease in audio performance in both the digital domain, and perhaps more importantly, in the analogue domain when the data is eventually converted back into its native form. The effect of jitter in digital audio systems is to reduce the resolution of the audio converter, raising the noise floor significantly. Audibly, this can mean the output signal is much less clean than the original analogue signal, which results in a fuzzy, flat sound.

With this firmly in mind, Wolfson Microelectronics designed the WM8805 and WM8804 digital interface transceivers to provide optimal PLL timing performance in S/PDIF applications. This enables class-leading jitter performance, and therefore vastly improved system tolerance to timing artefacts not fully covered by the various digital interface standards.

## **JITTER IN DIGITAL AUDIO SYSTEMS**

Despite the inherent advantages of digital data in terms of insensitivity to noise, distortion and crosstalk, one downside to using digital data is the introduction of jitter. Jitter is effectively the difference in time between when an event should happen, and when it does happen - for example a delta between ideal sampling instant, and actual sampling instant.

Jitter can affect clock signals, data signals, or both, and if allowed to pass unchecked through an audio system, it can lead to very poor audio performance – the introduction of errors, high distortion, and eventually the complete loss of lock.

Jitter can introduce problems in two areas of the audio system – at the digital interface, where it can cause a loss of lock and data corruption; and at the audio converter, where sampling jitter can induce errors, distortion and out of band noise.

It is therefore very important to minimise the amount of jitter created and propagated within a digital audio system. Wolfson Microelectronics' audio converters are highly insensitive to clock jitter, and the new family of S/PDIF transceivers exhibit excellent jitter performance, as detailed in the remainder of this paper.

## **SPECIFICATION OF JITTER**

Jitter in audio systems is specified in terms of the Unit Interval (UI), which is the smallest period of time for one bit of data at a given sampling rate. For an S/PDIF signal at 48kHz, one UI is equivalent to 163ns.

The key jitter metrics in assessing an S/PDIF transceiver are jitter tolerance and intrinsic jitter. These allow designers to measure the amount of jitter a device will introduce into their system, and the amount of jitter with which a device can operate before failing.

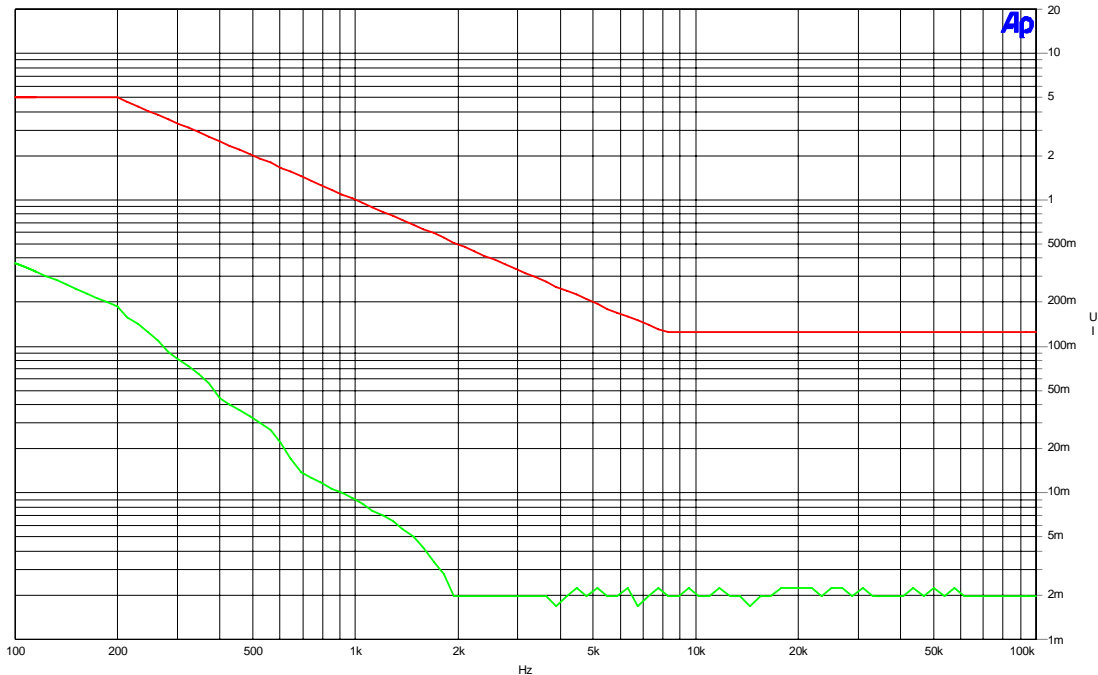
- Jitter tolerance – the amount of jitter the receiver should tolerate before losing lock
  - Specified at various frequencies:
  - 10UI below 5Hz
  - 0.25UI between 200Hz and 400kHz
  - 0.2UI above 400kHz
  
- Intrinsic jitter – the maximum jitter introduced by the transceiver itself
  - Specified as 0.05UI

The WM8804/5 excels in meeting and exceeding these performance metrics. Notably, the intrinsic jitter of the WM8805 is measured at 50ps, and the jitter rejection frequency of the onboard PLL is 100Hz. This can be directly compared with competitive S/PDIF solutions available today, with intrinsic jitter in the region of 150ps, and jitter rejection frequency greater than 20kHz.

The point of this illustration is that competitive solutions do little to attenuate jitter. An audio system including today's generation of S/PDIF transceivers cannot attenuate jitter on incoming signals, and adds a significant level of jitter to the overall system. This makes it very difficult to design a system to pass industry standard specifications.

## JITTER TOLERANCE

Figure 2 shows a jitter tolerance template of jitter vs. frequency, with a measurement of the WM8805 shown in comparison. An AES template has been used instead of IEC-60958-3 because of the availability of this template in the test equipment.

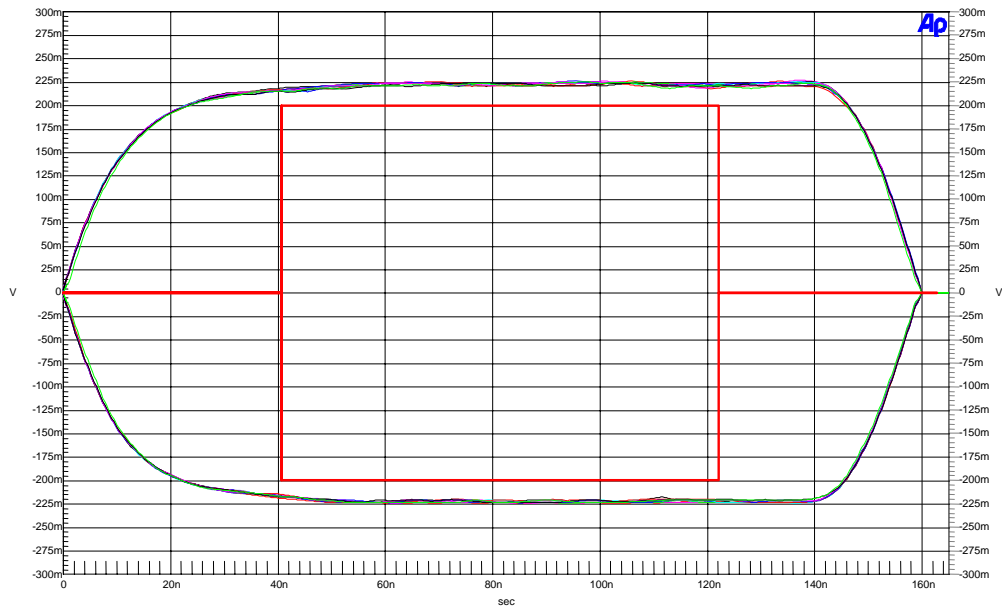


**Figure 2 Jitter Tolerance**

It is obvious that the WM8805 significantly exceeds the S/PDIF specification over the band of operation, tolerating far more jitter than is demanded by IEC60958-3. However, as previously discussed, merely meeting standards is not enough to guarantee overall system performance.

Figure 3 shows an eye diagram of the output of the WM8805 when the input is being stimulated with increasing amounts of jitter at 1kHz from 0UI to 500mUI in 50mUI steps. The Y-axis shows the output amplitude, and the X-axis shows the eye opening in time. The template is again taken from the AES3 specification.

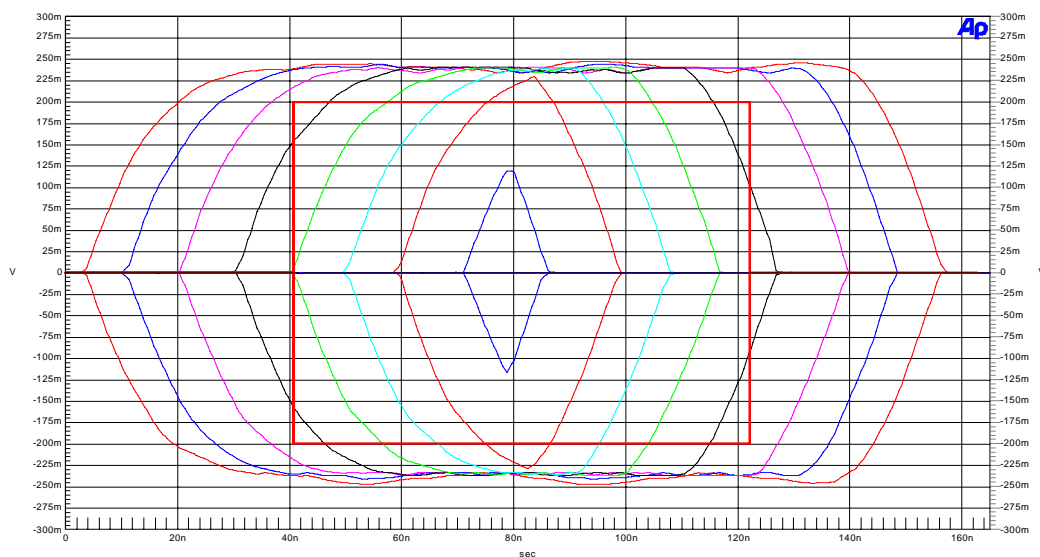
Note that the WM8805 easily passes this test with input jitter levels up to 500mUI. In fact, it can be shown that the WM8805 tolerates jitter up to 7UI, significantly more than can reasonably be expected in real audio systems.



**Figure 3 WM8805 Eye Diagram**

The performance of the WM8804/5 can be compared with that of a competitive solution in a like for like test. Note that the output level is slightly higher due to the competitive part operating from a 5V supply, compared with the WM8805's 3.3V supply.

It is obvious that this competitive device is not at all robust – it passes the test with a jitter input of 50mUI and 100mUI, but fails the IEC60958-3 template with a jitter input greater than or equal to 150mUI. The competitor's transceiver loses lock entirely with jitter input greater than 350mUI. This device may be able to handle controlled test signals, but it is highly likely that such a part will have difficulty coping with real-world S/PDIF signals. Such performance will have a significant impact on the final quality, or even the availability, of the output signal.



**Figure 4 Competitive Eye Diagram**

## INTRINSIC JITTER

Figure 5 shows the intrinsic jitter of the WM8805 and Figure 6 shows the jitter present at the output when 5UI of jitter is applied at 1kHz, around 50ps in both cases. This serves to show that the DUT jitter output is very low, and is relatively unaffected by the level of jitter applied at the input.

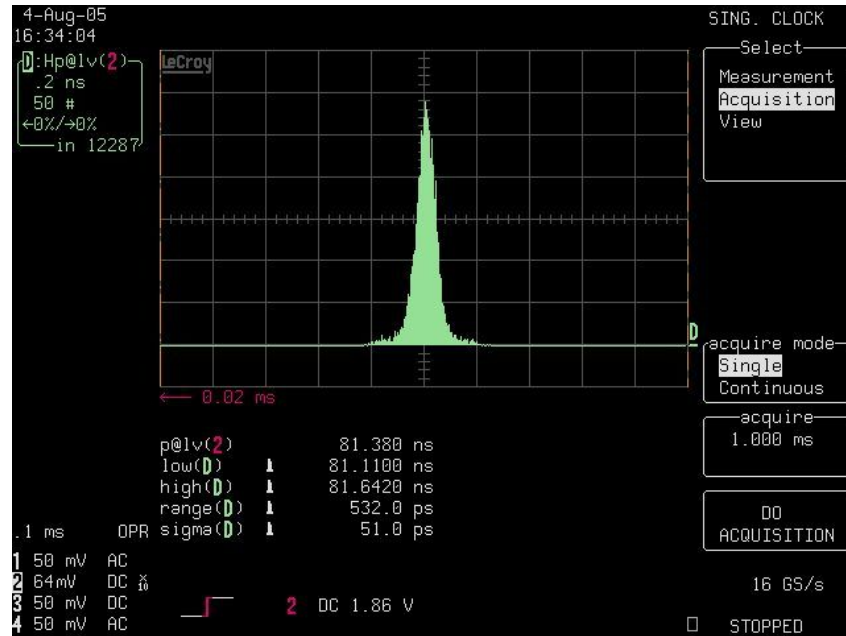


Figure 5 WM8805 Intrinsic Jitter

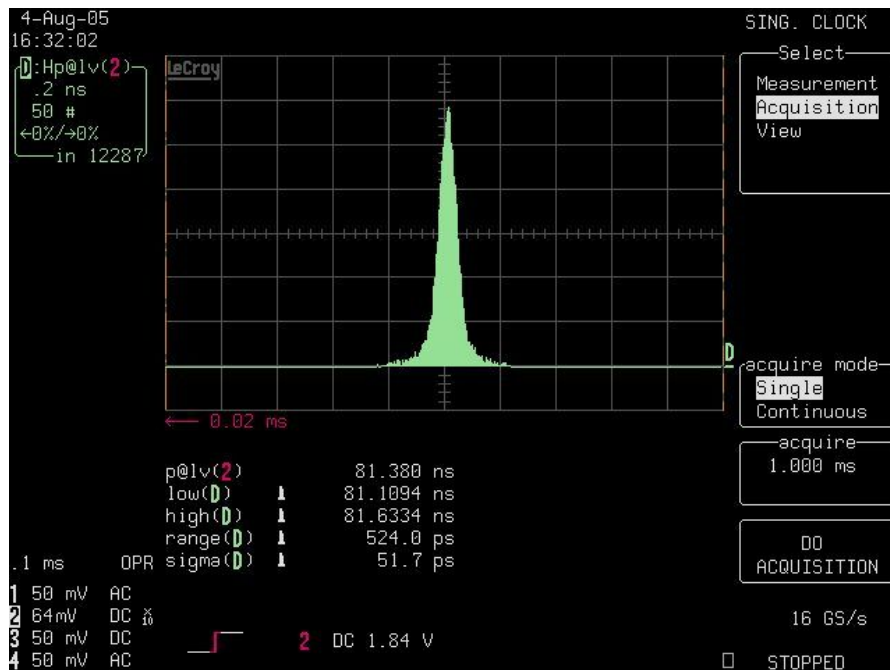


Figure 6 WM8805 5UI Jitter

While the competitive S/PDIF transceiver exhibits similar static performance, Figure 7 shows a stark contrast in performance between the WM8805 and competitive parts.

When stimulated with the same level of jitter as for Figure 6, the competitive part's output jitter increases to 334ps. It is obvious that the competitive transceiver does little to attenuate the input jitter.

This does not necessarily contravene the S/PDIF specifications, but it can and does lead to system-level problems in performance, and again illustrates the point that merely meeting specifications is not enough to guarantee high performance.

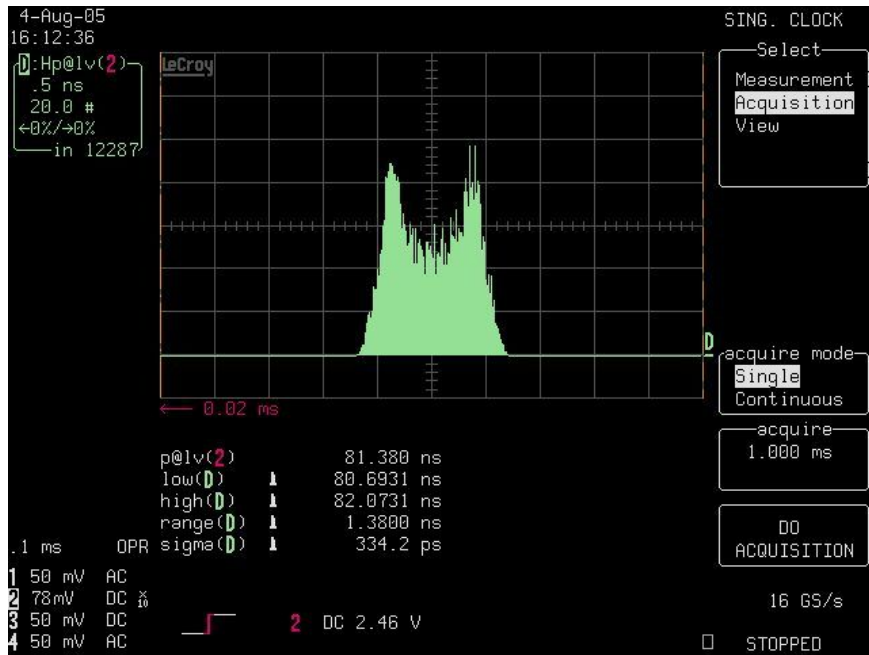


Figure 7 Competitive 5UI Jitter



## CONCLUSIONS

It has been demonstrated that meeting industry standards is not necessarily enough to guarantee error-free system operation and excellent performance in digital audio networking applications.

- Compliance with IEC60958 and/or AES3 may mean adequate performance in isolation, but can lead to problems in overall system operation.
- Of particular importance are timing parameters such as jitter tolerance and intrinsic jitter; both can have a serious impact on audio quality in the digital and analogue domain if products are not robust enough to handle real-world, as opposed to theoretical, implementation issues.

Wolfson's established portfolio of audio converters have long been proven to be highly insensitive to sampling jitter, and the WM8804 and WM8805 digital interface transceivers have now been shown to provide excellent interface jitter performance.

- In direct comparison with widely-used competitive S/PDIF transceivers, the WM8804 and WM8805 have exhibited an extremely high level of immunity to jitter, allowing the devices to effectively de-jitter clock and data signals for further processing within the audio system.
- This has a direct and significant impact on the audio experience of the product's end-user.

The high level of performance combined with the flexibility of the WM8804/5 make it easy for designers to incorporate these devices into digital audio systems. WM8804 and WM8805 are an excellent addition to Wolfson's portfolio of audio products, combining the level of performance required in the professional audio market with the competitiveness associated with the consumer electronics space.

## REFERENCES

1. [FRAND04] – Frandsen, Christian; Lave, Morten; "Plug and Play? An investigation into problems and solutions of digital audio networks"; AES Convention Paper, May 2004.
2. [SCHUT] – Schut, Peter; "Why jitter matters in high resolution digital audio systems."
3. [ATKI90] – Atkinson, John; "Jitter, bits and sound quality"; December 1990.

## SUPPLEMENT

### WM8805 8:1 S/PDIF DIGITAL INTERFACE TRANSCEIVER

The WM8805 is an eight-input, one-output, IEC60958-3-compliant S/PDIF transceiver. In addition to the jitter performance discussed previously, the WM8805 offers the following benefits and features:

Figure 8 shows the WM8805 block diagram.

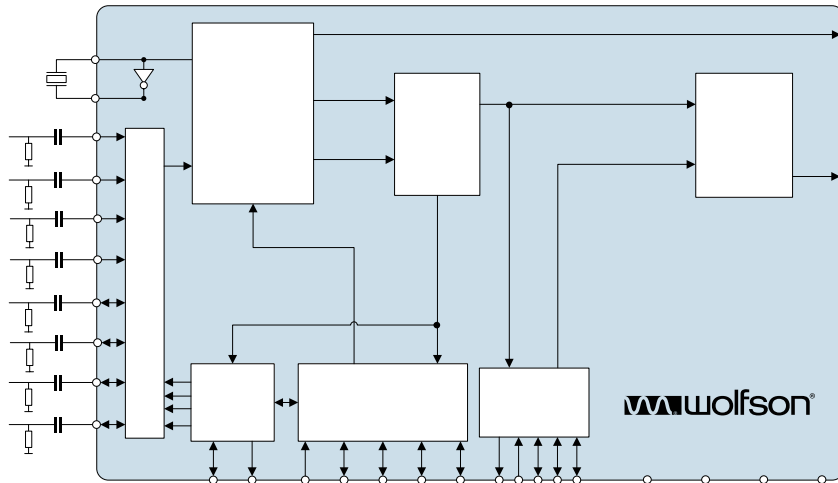


Figure 8 WM8805 Block Diagram

#### KEY FEATURES

- S/PDIF (IEC60958-3) compliant
- Advanced jitter attenuating PLL
  - Low intrinsic period jitter of 50 ps RMS
  - Jitter attenuation frequency of 100Hz
- S/PDIF recovered clock using PLL, or stand alone crystal derived clock generation
- Supports 10 – 27MHz crystal clock frequencies
- 2-wire / 3-Wire Serial Control Interface with Read-back, or Hardware Control Interface
- Programmable Audio Data Interface Modes:
  - I<sup>2</sup>S, Left, Right Justified or DSP
  - 16/20/24 bit Word Lengths
- 8 channel receiver input and 1 channel transmit output

- Auto frequency detection / synchronisation
- Selectable output status data bits
- Up to 8 configurable GPO pins
- De-emphasis flag output
- Non-audio detection including DOLBY™ and DTS™
- Channel status changed flag
- Configurable clock distribution with selectable output MCLK rate of 512fs, 256fs, 128fs and 64fs
- 2.7 to 3.6V Digital and PLL Supply voltages
- 28 pin SSOP package

#### APPLICATIONS

- Surround Sound AV Processors and Hi-Fi systems
- Music industry applications
- DVD-P/DVD-RW
- Digital TV

## WM8804 1:1 S/PDIF DIGITAL INTERFACE TRANSCEIVER

The WM8804 is a one-input, one-output S/PDIF transceiver, offering the same high level of performance as the WM8805, in an even more competitive 20-SSOP package. Figure 9 shows the WM8804 block diagram.

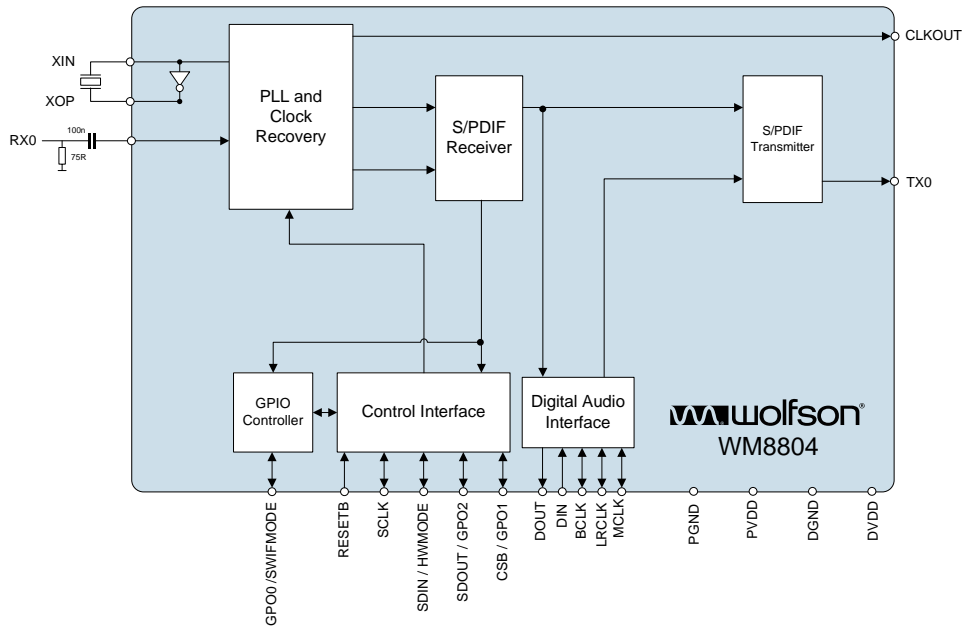


Figure 9 WM8804 Block Diagram

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